ABSTRACT

The present invention provides a circuit for processing integer data, especially for graphic applications, comprising:

- a multiplier unit for multiplying integer data words, of 8 bits or multiples thereof in which unit a pipeline forms part and the word length of which is adjustable for the multiplication to be performed in accordance with the multiple of 8 bits for multiplying;
- an arithmetic logic unit (ALU) for performing arithmetic operations on integer data words of 8 bits or multiples thereof, the word length of which is adjustable in accordance with the multiple of 8 bits for processing;
- a register unit provided with at least two registers for storage therein for some time of integer data words of a multiple of 8 bits on which the operation and/or pipeline multiplication has to be performed; and
- a bus structure which comprises a number of separate buses and which effects the transport of integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit.